Claims

1. *(Currently amended)* A magnetic random access memory (MRAM) ~~with stackable architecture~~ comprising:

a substrate;

a first memory cell column extending perpendicularly from the substrate and comprising a plurality of stacked magnetic memory cells electrically coupled to ~~and stacked on top of~~ each other, each magnetic memory cell configured to store data;

~~a first conductive word line electrically coupled to the first memory column; and~~

a first bit line column extending perpendicularly from the substrate ~~horizontally disposed from~~ and ~~parallel~~ adjacent to but electrically isolated from the first memory cell column, the first bit line column ~~electrically isolated from the first word line and~~ comprising a plurality of stacked conductive bit lines electrically isolated from ~~the first memory column and from~~ each other, each bit line ~~the first bit line column~~ in the first bit line column being associated with a memory cell in the adjacent memory cell column and positioned close enough to its associated memory cell such that an electric current passing through ~~one of the plurality of bit lines~~ a bit line will produce a magnetic field affecting ~~one of the plurality of magnetic~~ the memory cell associated with that bit line ~~cells~~; and

a first conductive word line electrically coupled to the first memory cell column and electrically isolated from the first bit line column.

Claim 2. *(Canceled)*

3. *(Currently amended)* The MRAM of claim 1 wherein ~~each of~~ the ~~plurality of~~ bit lines in the first bit line column are aligned parallel to one another and ~~is~~ perpendicular to the first memory cell column.

4. *(Currently amended)* The MRAM of claim 1 further comprising:

an electrical insulator located ~~positioned~~ between the first bit line column and the first memory cell column.

5. *(Currently amended)* The MRAM of claim 1, further comprising:

a second bit line column extending perpendicularly from the substrate and electrically isolated from the first conductive word line, the second bit line column comprising a plurality of stacked conductive bit lines electrically isolated from each other, the bit lines in the second bit line column being aligned parallel to one another and to the bit lines in the first bit line column, the first and second bit line columns being located on opposite sides of the first memory cell column ~~and configured to carry electric current during a memory read and a memory write~~; and

an electrical insulator located between the second bit line column and the first memory cell column.

Claims 6-9. *(Canceled)*

10. *(Currently amended)* The MRAM of claim 5 9 further comprising:

a second memory cell column extending perpendicularly from the substrate and electrically coupled to the first conductive word line and comprising a plurality of stacked magnetic memory cells electrically coupled ~~and adjacent~~ to each other, each memory cell configured to store data, the second memory cell column being parallel to the first memory cell column and adjacent to the first bit line column.

11. *(Currently amended)* The MRAM of claim 10 further comprising:

a second conductive word line parallel to the first conductive word line; and

a third memory cell column extending perpendicularly from the substrate parallel to the first memory cell column and electrically coupled to the second conductive word line and comprising a plurality of magnetic memory cells electrically coupled ~~and adjacent~~ to each other, each memory cell configured to store data.

Claim 12. *(Canceled)*

13. *(Currently amended)* The MRAM of claim 11 ~~12~~ wherein the third memory cell column is located ~~positioned~~ between the first and second bit line columns.

14. *(Currently amended)* The MRAM of claim 11 wherein one of the plurality of memory cells in the first memory cell column is configured to store data when electric current flows through the first conductive word line into the first memory cell column and electric current flows through one of the ~~plurality of~~ bit lines in the second bit line column.

15. *(Currently amended)* The MRAM of claim 14 wherein one of the plurality of memory cells in the first memory cell column is further configured to store data when electric current flows through one of the ~~plurality of~~ bit lines in the first bit line column.

16. *(Currently amended)* The MRAM of claim 15 wherein the direction of current flowing through one of the ~~plurality of~~ bit lines in the first bit line column is opposite the direction of current flowing through one of the ~~plurality of~~ bit lines in the second bit line column.

17. *(Currently amended)* The MRAM of claim 15 wherein the direction of current flowing through one of the ~~plurality of~~ bit lines in the first bit line column is the same as the direction of current flowing through one of the ~~plurality of~~ bit lines in the second bit line column.

18. *(Currently amended)* The MRAM of claim 1, each of the ~~plurality of~~ memory cells in the first memory cell column further comprising:

a readout layer configured to have a magnetic polarization; and

a storage layer coupled to the readout layer and configured to have a magnetic polarization, the storage layer having a higher coercivity than the readout layer.

19. *(Currently amended)* The MRAM of claim 18, wherein the readout layer and the storage layer are configured to align their magnetic polarizations with a magnetic field generated by the electric current in one of the ~~plurality of~~ bit lines during memory write, and the readout layer is configured to align its magnetic polarization with a magnetic field generated by the electric current in one of the ~~plurality of~~ bit lines during memory read.

20. *(Currently amended)* A magnetic random access memory (MRAM) ~~with stackable architecture~~ comprising:

a substrate;

a word line configured to carry electric current;

a stack of magnetic memory cells extending perpendicularly from the substrate and ~~cell~~ electrically coupled to the word line, each memory cell ~~and~~ configured to store data; and

a stack of bit lines extending perpendicularly from the substrate adjacent to the stack of memory cells ~~line~~, each bit line being magnetically coupled to an adjacent associated ~~the~~ magnetic memory cell and electrically isolated from the word line, ~~the~~ each bit line configured to set a magnetic polarization within ~~the~~ itsadjacentassociated magnetic memory cell during a memory write operation and to set a magnetic polarization within ~~the~~ its adjacent associated magnetic memory cell during a memory read operation.

21. *(Currently amended)* The MRAM of claim 20 wherein ~~the~~ each bit line is further configured to reverse a magnetic polarization within ~~the~~ its adjacent associated magnetic memory cell during the memory read operation.

22. *(Currently amended)* A method of writing to magnetic random access memory (MRAM) with a word line, a magnetic memory cell electrically coupled to the word line, a switch electrically coupled to the memory cell, and a bit line magnetically coupled to, adjacent to and electrically isolated from the memory cell, the method comprising:

generating an electric current in the word line;

turning on the switch to direct current from the word line through the memory cell;

~~receiving an electric current in the magnetic memory cell;~~

generating a magnetic field around the bit line while current from the word line is passing through the memory cell to thereby align ~~; and aligning~~ a magnetic polarization within the magnetic memory cell according to the direction of the magnetic field.

23. *(Currently amended)* The method of claim 22 ~~further comprising:~~ wherein generating a magnetic field around the bit line to thereby align a magnetic polarization within the magnetic memory cell comprises:

aligning a magnetic polarization within a readout layer in the magnetic memory cell according to the direction of the magnetic field; and

aligning a magnetic polarization within a storage layer in the magnetic memory cell according to the direction of the magnetic field, the storage layer coupled to the readout layer and having a higher coercivity than the readout layer.

24. *(Original)* The method of claim 23, further comprising:

generating an electric current; and

electrically lowering the switching field of the memory cell.

25. *(Original)* The method of claim 23, further comprising:

heating the memory cell; and

lowering the switching field of the memory cell.

26. *(Original)* The method of claim 23, further comprising:

generating an electric current; and

magnetically lowering the switching field of the memory cell.

27. *(Currently amended)* A method of reading from a magnetic random access memory (MRAM) with a word line, a magnetic memory cell electrically coupled to the word line, and a bit line magnetically coupled to, adjacent to and electrically isolated from the magnetic memory cell, the method comprising:

generating a magnetic field in a first direction around the bit line to thereby align ~~;aligning~~ a magnetic polarization within the memory cell according to ~~the~~ said first direction of the magnetic field;

measuring a resistance of the memory cell;

generating a magnetic field in a second direction opposite said first direction around the bit line to thereby reverse ~~reversing~~ the magnetic polarization within the magnetic memory cell; and

measuring the resistance of the magnetic memory cell with said reversed magnetic polarization.

28. *(Currently amended)* The method of claim 27 wherein measuring the resistance of the magnetic memory cell comprises ~~further comprising~~:

generating an electric current in the word line; and

receiving an electric current in the magnetic memory cell.

Claim 29. *(Canceled)*

30. *(Currently amended)* The method of claim 27 ~~further comprising:~~ wherein generating a magnetic field in a first direction around the bit line to thereby align a magnetic polarization within the memory cell comprises aligning a magnetic polarization within a readout layer in the magnetic memory cell ~~according to the direction of the magnetic field~~; and wherein generating a magnetic field in a second direction opposite said first direction around the bit line to thereby reverse the magnetic polarization within the magnetic memory cell comprises reversing the magnetic polarization within the readout layer.

31. *(Currently amended)* A method of reading from a magnetic random access memory (MRAM) with a word line, a magnetic memory cell electrically coupled to the word line, and a bit line magnetically coupled to, adjacent to and electrically isolated from the memory cell, the method comprising:

measuring the resistance of the magnetic memory cell;

generating a magnetic field around the bit line to thereby reverse ~~; reversing~~ a magnetically pre-existing polarization within the magnetic memory cell according to the direction of the magnetic field; and

measuring the resistance of the memory cell.

Claim 32. *(Canceled)*

33. *(Original)* A magnetic random access memory (MRAM) with stackable architecture comprising:

a memory cell comprising:

a storage layer with high-coercivity configured for storing information;

a thin insulating layer coupled to the storage layer and configured to form a magnetic tunneling junction (MTJ); and

a readout layer with low-coercivity coupled to the thin insulating layer and configured to provide a relative readout for determining the magnetization of the storage layer.

34. *(Original)* The MRAM of claim 33 wherein the storage and readout layers further comprise a plurality of CoPt layers, wherein the number of CoPt layers determines the relative coercivity between the storage and readout layers.

35. *(Original)* The MRAM of claim 34 further comprising:

a first bit line magnetically coupled to and electrically isolated from the magnetic memory cell; and

a second bit line magnetically coupled to and electrically isolated from the magnetic memory cell and parallel to the first bit line, wherein the first and second bit lines are configured to generate a magnetic field at the location of the magnetic memory cell by conveying electric current in opposite directions.

36. *(Original)* The MRAM of claim 34 further comprising:

a first bit line magnetically coupled to and electrically isolated from the magnetic memory cell; and

a second bit line magnetically coupled to and electrically isolated from the magnetic memory cell and parallel to the first bit line, wherein the first and second bit lines are configured to generate a magnetic field at the location of the magnetic memory cell by conveying electric current in the same direction.

37. *(Original)* The MRAM of claim 36 wherein the magnetic memory cell is between the first and second bit lines.

38. *(Original)* The MRAM of claim 36 further comprising:

a cladding layer coupled to the storage layer and configured to magnetically couple the first and second bit lines to the magnetic memory cell, wherein the magnetization of the storage layer switches through anti-parallel magnetic coupling of the storage layer and the cladding layer.

39. *(Original)* The MRAM of claim 38 further comprising:

a first CuTa layer coupled to the memory cell;

a second CuTa layer coupled to the first bit line; and

a third CuTa layer coupled to the second bit line, the first, second and third CuTa layers configured to control the resistance of the magnetic memory cell, first and second bit lines.

40. *(Currently amended)* A magnetic random access memory (MRAM) with stacked memory ~~stackable~~ layers~~, the MRAM having a plurality of conductive word lines,~~ comprising:

a substrate;

a first memory layer on the substrate and comprising: (a) a first plurality of magnetic memory cells aligned in a first row, each of the first plurality of memory cells separated by an insulator and electrically isolated from each other and configured to store information~~, each magnetic memory cell coupled to one of each of the plurality of word lines~~; ~~and~~ (b) a first conductive bit line parallel to, horizontally disposed from, and electrically isolated from the first row, the first bit line configured to select from the first plurality of magnetic memory cells, wherein the first bit line is close enough to be magnetically coupled to the first row; and (c) a second conductive bit line parallel to and electrically isolated from the first row, the first row being located between the first and second bit lines, the second bit line configured, in conjunction with the first bit line, to select from the first plurality of magnetic memory cells, wherein the second bit line is close enough to be magnetically coupled to the first row;

a second memory layer on the first memory layer and comprising (d) a second plurality of magnetic memory cells aligned in a second row above the first row, each of the second plurality of memory cells separated by an insulator and electrically isolated from each other and configured to store information, each of the memory cells in the second row being stacked on and aligned with a corresponding memory cell in the underlying first row to form a memory cell column on the substrate; (e) a third conductive bit line above the first conductive bit line and parallel to, horizontally disposed from, and electrically isolated from the second row, the third bit line being stacked on and aligned with the underlying first bit line to form a first bit line column

on the substrate, the third bit line configured to select from the second plurality of magnetic memory cells, wherein the third bit line is close enough to be magnetically coupled to the second row; and (f) a fourth conductive bit line above the second conductive bit line and parallel to and electrically isolated from the second row, the second row being located between the third and fourth bit lines, the fourth conductive bit line being stacked on and aligned with the underlying second bit line to form a second bit line column on the substrate, the fourth bit line configured, in conjunction with the third bit line, to select from the second plurality of magnetic memory cells, wherein the fourth bit line is close enough to be magnetically coupled to the second row; and

a plurality of conductive word lines above the second layer and aligned orthogonal to and electrically isolated from the bit lines, each conductive word line being electrically coupled to a respective memory cell column.

Claims 41-46. *(Canceled)*

47. *(Currently amended)* A method of manufacturing a ~~co-planar~~ magnetic random access memory ~~cell~~ (MRAM), comprising:

sequentially depositing a series of layers ~~a plurality of magnetic memory cells~~ on a dielectric surface; and

~~depositing a plurality of bit lines on a dielectric surface simultaneously with the depositing of the plurality of memory cells.~~

thereafter patterning the deposited layers to simultaneously form a plurality of parallel rows of memory cells and a plurality of conductive bit lines parallel to the memory cell rows.